Case Docket No.PHA 1306

THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor(s):
HAIDEH KHORRAMABADI

For: WIRELESS RECEIVER WITH OFFSET COMPENSATION USING FLASH-ADC

ENCLOSED ARE

[X] 11 sheets of [X] informal [ ] formal drawings.
[X] An assignment of the invention to PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
[X] A fully executed Declaration.
[ ] An unsigned Declaration.
[ ] A certified copy of application Serial No. .
[X] Associate Power of Attorney.
[ ] Preliminary Amendment.
[ ] Information Disclosure Statement and Form PTO-1449.
[ ] Citation of Related Cases.

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $770.00
Total Claims	15 - 20 =		X $22 =	
Independent Claims	4 - 3 =	1	X $80 =	80.00
Multiple Dependent Claims, if any			$260 =	
TOTAL FILING FEE			=	$850.00

Please charge Deposit Account No. 14-1270 in the amount of $850.00. The Commissioner is hereby authorized to charge any fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ] Amend the specification by inserting before the first line the sentence: - This is a continuation-in-part of application Serial No. , filed

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March 20, 1997

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     (FILE 'USPAT' ENTERED AT 11:47:56 ON 02 AUG 1998)
L1          4347 S SWITCH####(3W)ZERO##
L2         16886 S SWITCH####(3A)GROUND###
L3         70857 S ANALOG##(3W)DIGITAL OR ADC
L4        137766 S FEEDBACK# OR (FEED OR FED)(1W)BACK#
L5             2 S L3(P)L1(P)L2 AND L3
L6             1 S 4654584/PN
L7             3 S (SETTING OR FIXED OR FIXING OR MAINTAIN###)(7W)L1(P)L2
L8             1 S (SETTING OR FIXED OR FIXING OR MAINTAIN###)(7W)L4(9W)ZER
O##
L9            21 S (SUBTRACT#### OR DIFFERENCE OR ADDING)(8A)(AIN OR VIN OR
 (A
L10           14 S L9 AND L4
L11            2 S L9(P)L4
L12            1 S L9 AND (L1 OR L2)
L13            0 S SWITCH####(3A)L4(W)LOOP(9W)ZERO##(10W)(GROUND## OR REFER
ENC
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data search

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his


     (FILE 'USPAT' ENTERED AT 06:40:41 ON 04 MAR 1998)
L1         67718 S ADC OR ANALOG##(3W)DIGITAL
L2         47920 S DIGITAL(3W)ANALOG## OR DAC
L3        441861 S OFFSET# OR CALIBRAT?  OR ERROR#
L4         20126 S L1 AND L2 AND L3
L5        755081 S REGISTER# OR STOR? OR BUFFER
L6           289 S L1(9W)L5(10W)L2
L7           165 S L3 AND L6
L8        117704 S FEEDBACK# OR FEDBACK OR FEED(W)BACK#
L9            57 S L7 AND L8
L10            6 S (3988689 OR 3636463 OR 4308504 OR 4301121 OR 4395681 OR
435
L11            5 S L3 AND L10
L12         5130 S L1(7W)L5
L13         3918 S L5(7W)L2
L14          850 S L12 AND L13
L15          293 S L14 AND L8
L16          377 S L12(P)L13
L17          111 S L8 AND L16
L18          103 S L1(P)L2(P)L3(P)L5(P)L8
L19           24 S L18 AND 341/CLAS
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his

(FILE 'USPAT' ENTERED AT 10:36:58 ON 06 MAR 1998)

L1	67718	S	ANALOG##(3W)DIGITAL OR ADC
L2	685827	S	REGISTER OR STOR?
L3	388310	S	OFFSET# OR ERROR#
L4	47920	S	DIGITAL(3W)ANALOG## OR DAC
L5	117	S	L2(9W)L4(9W)AMPLIF?
L6	65	S	L3 AND L5
L7	3076	S	L4(5A)AMPLIF?
L8	4661	S	L1(5A)L2
L9	279	S	L7 AND L8
L10	202	S	L3 AND L9
L11	33711	S	RADIO FREQUENCY
L12	5	S	L10 AND L11
L13	30	S	L10 AND 341/CLAS

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     (FILE 'USPAT' ENTERED AT 16:11:43 ON 04 MAR 1998)
                SET PAGELENGTH 99
                SET AUHELP NONE
L1          15451 S FIX###(4W)(ANALOG## OR LEVEL OR INPUT)
L2          71919 S RADIO(W)FREQUENCY OR RF
L3           1186 S L1 AND L2
L4             35 S (ANALOG##(1W)PROCESSOR)(P)(ANALOG##(3W)DIGITAL OR ADC)(P)(D
L5              3 S L1 AND L4
L6              1 S L3 AND L4
L7          53919 S (COMPENSAT? OR CORRECT?)(8A)(OFFSET? OR ERROR#)
L8            220 S L7 AND L3
L9              6 S FIXED INPUT LEVEL
L10            61 S FIX###(1A)(ANALOG OR INPUT)(2A)LEVEL
L11             4 S L7 AND L10 AND L2
L12             0 S L4 AND L10
L13           508 S (CONTROLLING OR CONTROLLER)(4A)(ANALOG OR INPUT)(2A)LEVEL
L14            68 S L7 AND L13
L15             9 S L2 AND L14
L16         47323 S PRECURSOR

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     (FILE 'USPAT' ENTERED AT 15:14:51 ON 04 MAR 1998)
                SET PAGELENGTH 99
                SET AUHELP NONE
L1          67718 S ADC OR ANALOG##(3W)DIGITAL
L2          47920 S DIGITAL(3W)ANALOG## OR DAC
L3         638745 S OFFSET? OR CORRECT? OR ERROR# OR CALIBRAT?
L4          12815 S FIX##(3W)(INPUT OR LEVEL OR ANALOG##)
L5           7238 S (CONTROLLER OR CONTROLLING OR CONTROLLED)(6W)ANALOG##
L6            401 S L3(P)L2(P)(L4 OR L5)
L7            303 S L1 AND L6
L8             39 S AUDIO AND L7
L9          33711 S RADIO FREQUENCY
L10            19 S L7 AND L9

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5. 4,336,534, Jun. 22, 1982, Control generator for use in broadcast receiver including improved signal level indicator; Morio Kumagai, 345/39, 208; 455/159.2 [IMAGE AVAILABLE]

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Gilbert P. Hyatt, 3 02 [IMAGE AVAILABLE]

45. 4,476,420, Oct. 9, 1984, Circuit arrangement for synthesizing a sinusoidal position signal having a desired phase and high-resolution positioning system making use of the circuit arrangement; Teruo Asakawa, 318/608; 341/13 [IMAGE AVAILABLE]

46. 4,471,340, Sep. 11, 1984, Analog to digital converter; Bernard L. Lewis, 341/157, 118, 127 [IMAGE AVAILABLE]

47. 4,446,533, May 1, 1984, Stored program digital data processor; Richard J. Backhouse, 711/213; 364/922, 922.4, 926, 926.1, 926.5, 927.8, 928, 933.3, 933.61, 934, 934.71, 937.1, 937.2, 938, 938.3, 947, 947.6, 959.1, 960, 960.2, 964, 964.1, 965, 965.5, DIG.2 [IMAGE AVAILABLE]

48. 4,445,189, Apr. 24, 1984, Analog memory for storing digital information; Gilbert P. Hyatt, 364/600, 862; 365/45, 183; 446/302 [IMAGE AVAILABLE]

49. 4,428,070, Jan. 24, 1984, Dynamic circulation memory; Arthur H. M. van Roermund, et al., 365/222, 73 [IMAGE AVAILABLE]

50. 4,427,973, Jan. 24, 1984, A-To-D converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/134, 154; 377/54 [IMAGE AVAILABLE]

51. 4,400,690, Aug. 23, 1983, A-to-D Converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/134, 154 [IMAGE AVAILABLE]

52. 4,400,689, Aug. 23, 1983, A-to-D Converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/134; 331/57, 111; 341/154 [IMAGE AVAILABLE]

53. 4,388,611, Jun. 14, 1983, Electricity billing meter having unique A/D conversion system; James E. Haferd, 341/122; 327/78, 91; 341/169; 364/178, 179, 483, 487 [IMAGE AVAILABLE]

54. 4,322,819, Mar. 30, 1982, Memory system having servo compensation; Gilbert P. Hyatt, 365/45, 222 [IMAGE AVAILABLE]

55. 4,222,385, Sep. 16, 1980, Electronic heart implant; Richard J. Backhouse, 607/9; 364/916, 916.3, 922, 922.3, 922.4, 926, 926.1, 926.5, 927, 931, 933.3, 933.5, 933.8, 934, 934.1, 935, 935.2, 935.4, 935.6, 937.1, 937.2, 937.4, 938, 938.1, 938.3, 938.4, 939, 939.5, 942.7, 943.9, 943.91, 943.92, 944, 945.4, 945.7, 946.2, 946.6, 946.7, 947, 947.2, 947.3, 947.6, 948.4, 948.91, 949, 949.1, 950, 950.4, 953, 954, 954.1, 954.5, 955, 955.6, 957, 957.1, 960, 960.2, 960.4, 964, 965, 965.5, 965.7, 965.78, 965.8, 966, 966.6, 966.7, DIG.2 [IMAGE AVAILABLE]

56. 4,001,813, Jan. 4, 1977, Precision capacitance to digital conversion system; Henry R. Kosakowski, 341/172; 324/607 [IMAGE AVAILABLE]

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11. 5,563,597, Oct. 8, 1996, Switched-capacitor one-bit digital-to-analog converter with low sensitivity to op-amp **offset** voltage; Damien McCartney, 341/150, 126, 143 [IMAGE AVAILABLE]

12. 5,535,142, Jul. 9, 1996, Circuit arrangement for an inductive position indicator; Walter Mehnert, et al., 364/559; 33/708; 324/207.15, 207.17, 207.25 [IMAGE AVAILABLE]

13. 5,446,455, Aug. 29, 1995, Auto-calibrated current-mode digital-to-analog converter and method therefor; Todd L. Brooks, 341/145, 118 [IMAGE AVAILABLE]

14. 5,426,431, Jun. 20, 1995, Analog/digital converter; Kazuo Ryu, 341/158, 161 [IMAGE AVAILABLE]

15. 5,410,621, Apr. 25, 1995, Image processing system having a sampled filter; Gilbert P. Hyatt, 382/260; 364/724.011; 382/263 [IMAGE AVAILABLE]

16. 5,373,292, Dec. 13, 1994, Integration type D-A/A-D Conversion apparatus capable of shortening conversion processing time; Akira Yasuda, 341/108, 152, 164, 166 [IMAGE AVAILABLE]

17. 5,339,275, Aug. 16, 1994, Analog memory system; Gilbert P. Hyatt, 365/45, 183, 222, 230.06 [IMAGE AVAILABLE]

18. 5,334,952, Aug. 2, 1994, Fast settling phase locked loop; Steven L. Maddy, et al., 331/1A, 10, 14, 16, 17 [IMAGE AVAILABLE]

19. 5,231,627, Jul. 27, 1993, Apparatus for reading optically encoded soundtracks; Michael W. Paul, et al., 369/125, 120, 124 [IMAGE AVAILABLE]

20. 5,198,785, Mar. 30, 1993, Dual edge pulse width modulation system; Edward P. Jordan, 332/109; 327/176; 375/238 [IMAGE AVAILABLE]

21. 5,154,242, Oct. 13, 1992, Power tools with multi-stage tightening torque control; Koji Soshin, et al., 173/178; 73/862.23, 862.331; 81/469; 173/179, 180 [IMAGE AVAILABLE]

22. 5,136,568, Aug. 4, 1992, Tracking circuit for guiding a beam of light along data tracks of a recorded medium; Friedrich Fuldner, et al., 369/44.25, 44.29, 44.32, 44.34, 54 [IMAGE AVAILABLE]

23. 5,115,172, May 19, 1992, Phase locked loop speed control circuit for controlling speeds and relative positions of objects; Hiroshi Ishii, et al., 318/38; 388/911, 921 [IMAGE AVAILABLE]

24. 5,111,205, May 5, 1992, Digital-to-analog and analog-to-digital converters; Patrice P. Morlon, 341/156, 118, 145, 154, 159 [IMAGE AVAILABLE]

25. 5,053,983, Oct. 1, 1991, Filter system having an adaptive control for updating filter samples; Gilbert P. Hyatt, 364/724.03, 724.04, 724.18 [IMAGE AVAILABLE]

26. 5,014,055, May 7, 1991, Analog-to-digital converter and method of

use utilizing charge redistribution; Andrew G. F. Dingwall, et al., 341/159, 158 [IMAGE AVAILABLE]

27. 4,991,023, Feb. 5, 1991, Microprocessor controlled universal video monitor; Gary H. Nicols, 348/554; 345/213 [IMAGE AVAILABLE]

28. 4,967,197, Oct. 30, 1990, Error correction system for digital to analog converters; Yung-Chow Peng, 341/118, 131, 144 [IMAGE AVAILABLE]

29. 4,910,706, Mar. 20, 1990, Analog memory for storing digital information; Gilbert P. Hyatt, 365/45, 189.01, 222, 230.01; 968/900, DIG.1 [IMAGE AVAILABLE]

30. 4,761,636, Aug. 2, 1988, A-to-D converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/133; 323/281, 313, 907; 327/502, 564, 584; 341/134 [IMAGE AVAILABLE]

31. 4,710,865, Dec. 1, 1987, Control system for positioning an object using switching from a speed control mode to a position control mode with adjustable brain; Makoto Higomura, 364/167.01; 318/592, 594; 364/157, 182, 474.3 [IMAGE AVAILABLE]

32. 4,707,682, Nov. 17, 1987, A-to-D converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/134; 323/281, 313, 907; 341/155 [IMAGE AVAILABLE]

33. 4,686,655, Aug. 11, 1987, Filtering system for processing signature signals; Gilbert P. Hyatt, 367/59; 364/421, 602, 724.011, 728.03; 367/41, 43 [IMAGE AVAILABLE]

34. 4,647,903, Mar. 3, 1987, Successive approximation analog-to-digital converter; Kazuo Ryu, 341/136, 145, 154, 163 [IMAGE AVAILABLE]

35. 4,628,609, Dec. 16, 1986, Incremental measuring and machine control system; Heinz Rieder, et al., 33/707; 250/237G [IMAGE AVAILABLE]

36. 4,622,536, Nov. 11, 1986, Ratio independent cyclic A/D and D/A conversion using a reciprocating reference approach; Cheng-Chung Shih, et al., 341/108, 122, 136, 144, 158, 172 [IMAGE AVAILABLE]

37. 4,581,715, Apr. 8, 1986, Fourier transform processor; Gilbert P. Hyatt, 364/726.01 [IMAGE AVAILABLE]

38. 4,556,870, Dec. 3, 1985, A-To-d converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/119; 323/281, 313, 907; 341/134 [IMAGE AVAILABLE]

39. 4,553,221, Nov. 12, 1985, Digital filtering system; Gilbert P. Hyatt, 364/724.05, 421, 724.04, 728.03 [IMAGE AVAILABLE]

40. 4,553,213, Nov. 12, 1985, Communication system; Gilbert P. Hyatt, 332/185 [IMAGE AVAILABLE]

41. 4,547,766, Oct. 15, 1985, A-To-D converter of the successive-approximation type; Adrian P. Brokaw, et al., 341/134 [IMAGE AVAILABLE]

42. 4,523,290, Jun. 11, 1985, Data processor architecture; Gilbert P. Hyatt, 364/602, 862; 365/1, 222 [IMAGE AVAILABLE]

43. 4,516,177, May 7, 1985, Rotating rigid disk data storage device; William G. Moon, et al., 360/77.07, 77.02, 77.03, 77.05, 77.08 [IMAGE AVAILABLE]

44. 4,491,930, Jan. 1, 1985, Memory system using filterable signals;

16. 4,991,109, Feb. [redacted] 1991, Image processing syste[redacted]mploying pseudo-focal plane array; Rex J. Crookshanks, 345/207; 364/713; 382/254 [IMAGE AVAILABLE]

17. 4,968,970, Nov. 6, 1990, Method of and system for power line carrier communications; Eric LaPorte, 340/310.02, 310.03; 375/258 [IMAGE AVAILABLE]

18. 4,967,197, Oct. 30, 1990, Error correction system for digital to analog converters; Yung-Chow Peng, 341/118, 131, 144 [IMAGE AVAILABLE]

19. 4,965,867, Oct. 23, 1990, Offset compensation circuit; Masami Tsuchida, et al., 341/118, 143 [IMAGE AVAILABLE]

20. 4,817,022, Mar. 28, 1989, Method and apparatus for automatic offset compensation in parameter-sensing transducer systems; Eugene R. Jornod, et al., 364/571.03; 73/1.62, 765, 861.01; 364/558 [IMAGE AVAILABLE]

21. 4,720,992, Jan. 26, 1988, Calibration sequence and method for an electronic compass; Ronald F. Hormel, 73/1.76; 33/356, 361; 364/569, 571.04 [IMAGE AVAILABLE]

22. 4,714,341, Dec. 22, 1987, Multi-wavelength oximeter having a means for disregarding a poor signal; Kenji Hamaguri, et al., 356/41; 600/310 [IMAGE AVAILABLE]

23. 4,689,682, Aug. 25, 1987, Method and apparatus for carrying out television special effects; Richard A. Jackson, 348/578 [IMAGE AVAILABLE]

24. 4,588,983, May 13, 1986, Instantaneous gain changing analog to digital converter; Norman H. Strong, 341/167; 324/99D [IMAGE AVAILABLE]

25. 4,553,052, Nov. 12, 1985, High speed comparator circuit with input-offset compensation function; Kazukiyo Takahashi, 327/65, 69, 91, 215, 307 [IMAGE AVAILABLE]

26. 4,533,952, Aug. 6, 1985, Digital video special effects system; James W. Norman, III, 348/580, 590 [IMAGE AVAILABLE]

27. 4,375,595, Mar. 1, 1983, Switched capacitor temperature independent bandgap reference; Richard W. Ulmer, et al., 327/378; 323/314; 327/480, 539 [IMAGE AVAILABLE]

28. 4,355,285, Oct. 19, 1982, Auto-zeroing operational amplifier circuit; Stephen H. Kelley, et al., 330/9 [IMAGE AVAILABLE]

29. 4,282,515, Aug. 4, 1981, Analog to digital encoding system with an encoder structure incorporating instrumentation amplifier, sample and hold, offset correction and gain correction functions; Raymond B. Patterson, III, 341/118; 327/91; 341/122, 135, 165 [IMAGE AVAILABLE]

30. 3,810,031, May 7, 1974, INTEGRATED AMPLIFYING DEVICE HAVING LOW DRIFT AND METHOD OF COMPENSATING FOR THE DRIFT OF AN AMPLIFYING DEVICE; Robert Poujois, 330/6, 9, 253 [IMAGE AVAILABLE]

31. 3,685,048, Aug. 15, 1972, SELF-CALIBRATING ANALOG TO DIGITAL CONVERTER WITH PREDETERMINED TRANSFER CHARACTERISTICS; Ralph M. Pincus, 341/120, 169 [IMAGE AVAILABLE]

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1. 5,629,890, May 13, 1997, Integrated circuit system for analog signal storing and recovery incorporating read while writing voltage program method; Lawrence D. Engh, et al., 365/185.03, 45, 185.19, 185.29, 189.07 [IMAGE AVAILABLE]

2. 5,526,502, Jun. 11, 1996, Memory interface; Shinichi Yoshida, et al., 711/202; 345/515; 364/238.4, DIG.1 [IMAGE AVAILABLE]

3. 5,404,089, Apr. 4, 1995, PWM inverter controller with wave form memory; David F. Flanagan, et al., 318/811; 388/907.5 [IMAGE AVAILABLE]

4. 5,400,237, Mar. 21, 1995, PWM inverter controller with waveform memory; David F. Flanagan, et al., 363/41, 37, 95 [IMAGE AVAILABLE]

5. 5,311,085, May 10, 1994, Clocked comparator with offset-voltage compensation; Marcellinus J. M. Pelgrom, et al., 327/65, 94, 199; 330/253 [IMAGE AVAILABLE]

6. 5,283,531, Feb. 1, 1994, Demodulation apparatus incorporating adaptive equalizer for digital communication; Mutsumu Serizawa, et al., 329/316, 318, 327; 375/232; 455/303, 312 [IMAGE AVAILABLE]

7. 5,214,391, May 25, 1993, Demodulation apparatus having multipath detector for selecting a first or second demodulator; Mutsumu Serizawa, et al., 329/316, 318, 327; 375/232, 343, 349; 455/303, 312 [IMAGE AVAILABLE]

8. 5,205,316, Apr. 27, 1993, Air/water volume control system; Kearney L. Pruett, 137/209, 211.5 [IMAGE AVAILABLE]

9. 5,175,802, Dec. 29, 1992, Macro image processing system; Rex J. Crookshanks, 382/278, 281 [IMAGE AVAILABLE]

10. 5,168,398, Dec. 1, 1992, Head positioning control apparatus for a data storage device; Hiroyuki Kanda, et al., 360/78.04, 77.04; 369/44.29 [IMAGE AVAILABLE]

11. 5,159,282, Oct. 27, 1992, Demodulation apparatus incorporating adaptive equalizer for digital communication; Mutsumu Serizawa, et al., 329/316, 318, 327 [IMAGE AVAILABLE]

12. 5,125,008, Jun. 23, 1992, Method and apparatus for autoranging, quadrature signal generation, digital phase reference, and calibration in a high speed RF measurement receiver; Charles D. Trawick, et al., 375/349, 362, 373 [IMAGE AVAILABLE]

13. 5,045,685, Sep. 3, 1991, Analog to digital conversion on multiple channel IC chips; Llewellyn E. Wall, 250/208.1 [IMAGE AVAILABLE]

14. 4,991,127, Feb. 5, 1991, Offset and gain correction system for image data processing; Rex J. Crookshanks, 364/571.04; 348/262 [IMAGE AVAILABLE]

15. 4,991,111, Feb. 5, 1991, Real-time image processing system; Rex J. Crookshanks, 345/507; 364/713; 382/254 [IMAGE AVAILABLE]